"A Digital Signal Processor Based Vision System",

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A DIGITAL SIGNAL PROCESSOR BASED VISION SYSTEM

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ABSTRACT

A vision system was developed for image processing in the fields of robotics and product inspection. Taking advantage of the flexibility of a programmable DSP processor and being built around an industrial standard bus, the system can be configured in a number of ways allowing a wide spectrum of applications. Working under the control of an host computer the vision system, in its minimum configuration, is composed of two boards – a video acquisition display and transmission unit and an intelligent image processing unit – which are capable of handling images with 512x512 pixels with 256 grey levels per pixel. Standard basic operations on images such as arithmetic and logic operations, digital filtering and convolution are completed in a very short time after acquisition, due to the inclusion of a very fast digital signal processor in each processing unit. A modular design allows several intelligent image processing units to work in parallel increasing the total performance of the system.
The large quantity of data to deal with and the speed required by most applications precludes the use of conventional computers in the tasks of digital image processing. The need to make decisions in very short intervals of time, in areas like robotics, visual inspection and environment perception, led to a continuous research in developing specialized computer architectures, [1], [2] and [3], for image processing. In spite of their computational power these systems offer little flexibility and require a considerable effort in their programming, [3] and [4].

Figure 1: Block diagram of a VMEbus based vision system. The analog video signal of one out of four TV cameras is converted into digital form by an acquisition board and is made available, through a video bus, to several processing boards. A VME host computer controls the operation of the whole system.

The purposed vision system being based on a well established
computer bus benefits from the existence of a large number of hardware and software products and is easily integrated in existing industrial applications. As shown in Figure 1, the vision system is based on a video acquisition unit capable of transmitting the digitized video to a number of processing units which perform the intensive computation involved in image processing.

The described architecture, including a general purpose digital signal processor in the image processing units, allows the construction of a SIMD structure suitable for this type of processing without compromising flexibility. On the other hand, the modular approach taken in the design of the system permits its adaptation to particular applications. In its minimum configuration the vision system is composed of two VMEbus boards appearing as slaves to the host computer: a video acquisition display and transmission board and an intelligent image processing board. We now describe each of these units separately.

2. THE ACQUISITION DISPLAY AND TRANSMISSION BOARD

The video acquisition display and transmission board, shown in Figure 2, is a self-contained unit interfacing this system to standard black and white TV cameras using the CCIR norm and to conventional black and white or colour monitors. Up to four video inputs can be connected to the acquisition board which uses a flash 8-bit analog to digital converter to digitize the selected channel. Before being stored in the memory, the digitized sample passes through a look-up table of 256 entries allowing simple processing, such as binarization of an image, in real time. The look-up table is not dynamic but, using a 2K byte ROM, the host can select at any moment one out of eight previously fixed look-up tables. The display section of the board uses a conventional CRT controller and a colour look-up table which incorporates three 6-bit digital to analog converters to generate a RGB video
Each of the intelligent image processing boards used in the vision system consists of four parts (refer to Figure 3): a video input module, a TMS32020 microprocessor, a 256K bytes frame buffer and a VMEbus interface. The video input module uses both the data and the addresses appearing on the video bus to place an image, or a part of it, in memory. Under the command of the host computer the video input module may be configured to acquire images of different sizes (windows) and different resolutions. For example, the processing board may acquire an high resolution image of 256x256 pixels corresponding to the top right quarter of the original picture, or it may acquire a low resolution (but complete) image of 256x256 pixels. Windows with edges of 256 and 512 pixels are possible and in the former case they may be placed on a 128 pixel grid. Resolution can be low or high, corresponding to a full image sampled at 256x256 or 512x512 pixels, respectively.

Figure 3: A complete frame store for an image of 512x512 pixels and a dedicated TMS32020 DSP processor are the main parts of the intelligent processing unit.
In choosing a digital signal processor for this system a special
consideration was given to the capability of addressing a large
range of external memory as it is required in image processing.
The 16-bit TMS32020 processor, [5], with its 200ns instruction
cycle and its data address space of 64K words was chosen for this
application. The intelligence of the board is only local and the
dsp processor is totally controlled by the VME host computer. In
fact all the memory of the DSP processor, both program memory and
data or video memory, is RAM and appears in the address map of
the host which, for example, may halt the DSP processor, download
a program or a command, activate the reception of a picture
through the video bus and return control to the DSP processor for
execution of the command. The program memory of the TMS32020 can
be as large as 64K words but only 32K words are used in this
application. On the contrary all the data memory, 64K words as
well, is used by the processor: the first 32K words are for
general use and the second 32K words, or the top half of the data
memory, are used for video data as explained next.

The intelligent image processor board can store and process a
complete 8-bit 512x512 image, i.e. 256K pixels. This information
is physically stored on eight 32K bytes RAM chips which may be
accessed by three elements: the video bus, the VME host and the
TMS32020. For the first two elements this video memory is
organized as 128K words originating two pixels transfers per
access. For the DSP processor it is organized as 256K bytes in
eight pages of 32K bytes with only one of these pages being
present at a time on the top half of the DSP memory referred to
above. Note that when the TMS32020 addresses the video data on
the top of the memory it only finds 8-bit bytes in each location
instead of the usual 16-bit word. This is adequate for pixel
data. Another important aspect of the video memory organization
refers to the arbitration between the three sources of access.
The video bus has the highest priority having the whole memory
available during the total transfer of an image. The host
computer has the responsibility of halting the DSP processor
before making an access to the video memory, avoiding in this way
any conflicts in the access to the shared memory.
The VME interface module of the processing board permits the access to the video memory, the access to the TMS32020 program memory, the control of the video interface module and the control of a number of registers to operate the board. As it was already said the intelligent processing board is a slave for the VMEbus with the capability of generating interrupts mainly to signal completion of a command by the DSP processor. As in the case of the acquisition board the image processing unit is self-contained in the sense that it may work alone in a VME computer system. In this case images to process would be transferred through the VMEbus instead of the video bus and the power and flexibility of the DSP processor would be used with advantage.

4. SOFTWARE CONSIDERATIONS

Using and developing applications for this vision system is very facilitated by the existence of a number of commands which make the system hardware almost transparent to the user. Hardware dependent functions consist on a library of programs in 68000 assembler code which may be linked and integrated in application programs or called by high-level languages. These routines include test and initialization of the acquisition board, test and initialization of the processing board, look-up-table initialization, camera selection, size resolution and position of the image to be captured, acquisition and (or not) transmission of an image, moving images (memory, disk, ports, etc.) and, finally, image processing routines. Image processing routines are based on the TMS32020 processor and include filtering and convolution of an image, logic operations, Roberts and Sobel operators, zooming, and data compression. The code of the TMS32020 programs is contained in the 68000 routines and is downloaded into the intelligent boards under the control of the VME host computer. In this way the operation of the DSP processor may be ignored by the user who can think of the system as a conventional frame buffer occupying a predetermined space in the
signal with 256 colours from a palette of 256,144.

Figure 2: The general diagram of the acquisition display and transmission board.

The acquisition board has the capacity of storing two complete images of 512x512 pixels on its internal 512K bytes of RAM memory organized as two 256K bytes frame buffers — a useful facility during developing and testing stages to compare raw and processed images. Although the video memory is accessible by the CPU on a pixel basis, allowing image processing by the host, this is not the normal working situation. In fact a major feature of the board is the capability of transmitting, through a secondary bus, the digitized video which becomes available to the intelligent image processing boards that are connected to the system. When activated by the host, the transmitting section of the board sends two samples of video data and their corresponding addresses every 125ns. The video bus, which is constructed around uncommitted pins of the VMEbus P2 socket, has a very simple unidirectional structure since it carries the incoming camera picture in a usable form for the processing units.
address range of the VME computer.

5. REFERENCES