

# Remote lab for Stochastic Computing using Reconfigurable Logic

José Domingos Alves, Jorge Lobo

ISR - Institute of Systems and Robotics - University of Coimbra

DEEC - Department of Electrical and Computer Engineering, FCT, University of Coimbra

email: {jalves, jlobo}@isr.uc.pt

**Abstract**—In this interactive demonstration we show the basics of Stochastic Computing (SC) using a remote reconfigurable logic laboratory. A very simple web based approach is used to enable a remote access to a development board hosting a FPGA (Field Programmable Gate Array). The board switches and keys are virtualised with an online web form, and a webcam is used to provide feedback to the user. Recently, SC has been revisited and evaluated as a possible way of performing approximate probabilistic computations for artificial perception systems. Therefore, we provide the basic stochastic computing modules, so that any user can use them to build a stochastic computing circuit and go beyond software simulations, providing a remote hardware device to test real circuits at high clock speeds.

**Index Terms**—stochastic computing, remote lab, reconfigurable logic.

## I. INTRODUCTION

Stochastic Computing (SC), has been proposed by [1], [2] as an alternative number representation scheme, which provides higher tolerance to errors and more compact operators than conventional representation schemes, e.g. fixed-point and floating point binary representations. Essentially, stochastic, or telegraphic, signals are defined as generated by a memoryless continuous-time stochastic process producing two distinct values. A stochastic stream, according to [1], [2], is defined as a sequence of stochastic signals over time, where its value is defined as the number of ones over the total number of bits. Figure 1 shows a stochastic computing circuit realizing the arithmetic function  $z = X1X2X4 + X3(1 - X4)$ .

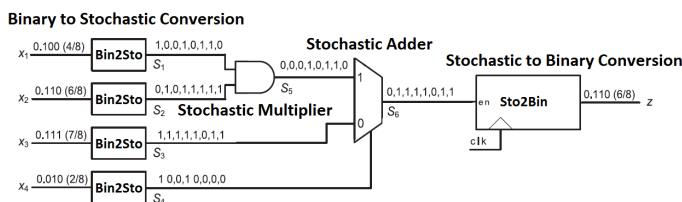


Fig. 1. Example of a stochastic computing circuit [3].

This demo showcases the implementation of the basic principles of Stochastic Computing on a remote hardware device, and how a user can build and test stochastic circuits.

## II. REMOTE LAB FOR STOCHASTIC COMPUTING

The remote lab connects an ALTERA DE2 FPGA board over the Internet, allowing it to be used as if the user is *in loco*, programming, testing and looking at it [4]. Figure 1 illustrates the basic concept of this remote lab. A web server that is accessible through the Internet is connected via USB to the FPGA JTAG port on the board, and a webcam for visual feedback connects to the server, conveying real-time results on the 16x2 LCD and the 7-segments displays [4]. The board switches and keys are virtualized with a webpage interface, with PHP dynamic functionalities that enabled the control of the remote hardware via the JTAG port.



Fig. 2. Concept of the reconfigurable logic remote laboratory board [4].

The main limitations of SC is that a linear increase in the precision of stochastic computations requires an exponential increase in the bit-stream length, sensitivity to temporal correlations, and limited dynamic range of the representation. Working with very long bit-streams can be time consuming when performing simulations, and dedicated hardware is a clear advantage. Therefore, this platform enables the designers to go beyond software simulations, providing a real hardware device for testing of real and high speed stochastic circuits.

## III. DEMO OF STOCHASTIC CIRCUITS ON REMOTE BOARD

The user steps to use this online platform for SC are:

- 1) Access the online remote lab (<http://lsd.deec.uc.pt>)
- 2) Register
- 3) Download the provided stochastic modules
- 4) Build stochastic circuit

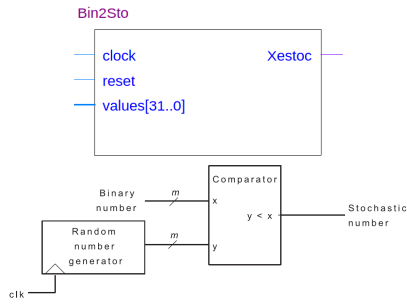


Fig. 3. Binary to stochastic converter module.

5) Test the stochastic circuit following the instructions given in [4]

#### A. Build and Test Circuit

To build a stochastic circuit, the users need to first download the stochastic modules. The provided modules for SC are:

- 1) Binary to Stochastic Converter (figure 3)
  - Random Number Generators (RNG)
    - Linear Feedback Shift Register
    - Ring Oscillators based RNG
  - Comparator
- 2) Stochastic to Binary Converter (figure 4)
- 3) Stochastic Multiplier and Stochastic Adder (figure 5)

The stochastic bit-stream generator (figure 3) is composed by a RNG and a Comparator. For the RNG two modules are provided: A Linear Feedback Shift Register (LFSR), and a hardware Random Number Generator. The LFSR has the advantage of its circuit simplicity, reproducibility and speed, but requires a seed. As alternative, we provide a high speed on-chip solution for generating random numbers using a RNG based on *jitter* sampling on ring oscillators requiring no seed [5]. The user can use it to replace the LFSRs or it can also be used to seed the LFSRs.

To build circuits capable of performing arithmetic operations on stochastic bit-streams, a Stochastic to Binary Converter (an up counter enabled by the input pin *cnt\_en* to count the number of ones in the stochastic bit-stream) (figure 4), a Stochastic Multiplier (using an AND gate), and a Stochastic Adder (using a Multiplexer) can also be downloaded. An example of such a stochastic computing circuit, realizing the arithmetic function  $z = X3(X1X2 + X4 + 1)$  is presented in figure 5.

To test a circuit using the remote hardware, the user should first follow the instructions given in [4].

#### IV. SUMMARY

The demo will show the basics of Stochastic Computing using a remote laboratory. The remote laboratory provides a

reconfigurable logic device (an Altera DE2 board hosting a Cyclone IV FPGA) to test real circuits. Besides the hardware

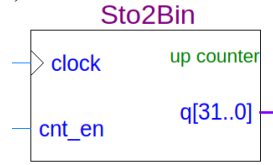


Fig. 4. Stochastic to binary conversion circuit module.

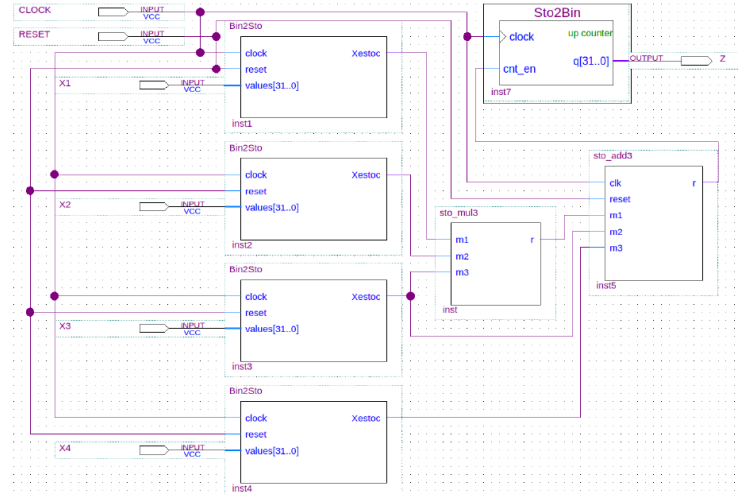


Fig. 5. Stochastic computing circuit built with the provided modules.

device, the demo also provides basic modules for Stochastic Computing and depending on user's interests and needs, complex stochastic computing circuits can be tested.

#### ACKNOWLEDGMENTS

The work leading to these results was partially supported by the European Commission collaborative FET project BAMBİ - Bottom-up Approaches to Machines dedicated to Bayesian Inference - FP7-ICT-2013-C, project number 618024 ([www.bambi-fet.eu](http://www.bambi-fet.eu)), and by the Institute of Systems and Robotics at Coimbra University.

#### REFERENCES

- [1] B. R. Gaines, "Techniques of identification with the stochastic computer," in *Proc. International Federation of Automatic Control Symposium on Identification, Prague*, 1967.
- [2] J. von Neumann, "Probabilistic logics and synthesis of reliable organisms from unreliable components," in *Automata Studies* (C. Shannon and J. McCarthy, eds.), pp. 43–98, Princeton University Press, 1956.
- [3] A. Alaghi and J. P. Hayes, "Survey of stochastic computing," *ACM Trans. Embed. Comput. Syst.*, vol. 12, pp. 92:1–92:19, May 2013.
- [4] J. Lobo, "Interactive demonstration of a remote reconfigurable logic laboratory for basic digital design," *International Journal of Online Engineering (iJOE)*, vol. 8, pp. 19–20, 2012.
- [5] B. Sunar, W. Martin, and D. Stinson, "A provably secure true random number generator with built-in tolerance to active attacks," *IEEE TRANSACTIONS ON COMPUTERS*, 2007.